

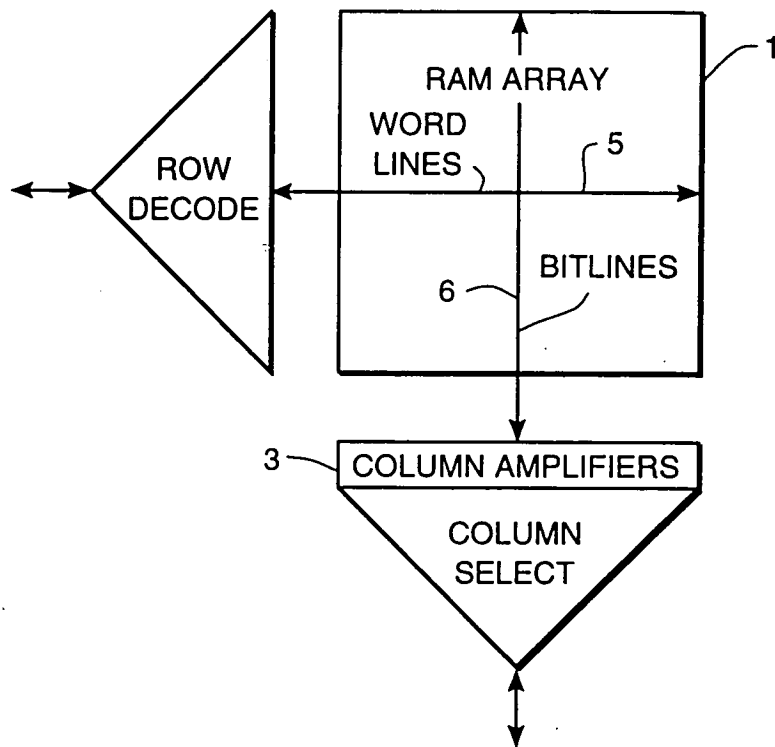
FIG 1

FIG 2

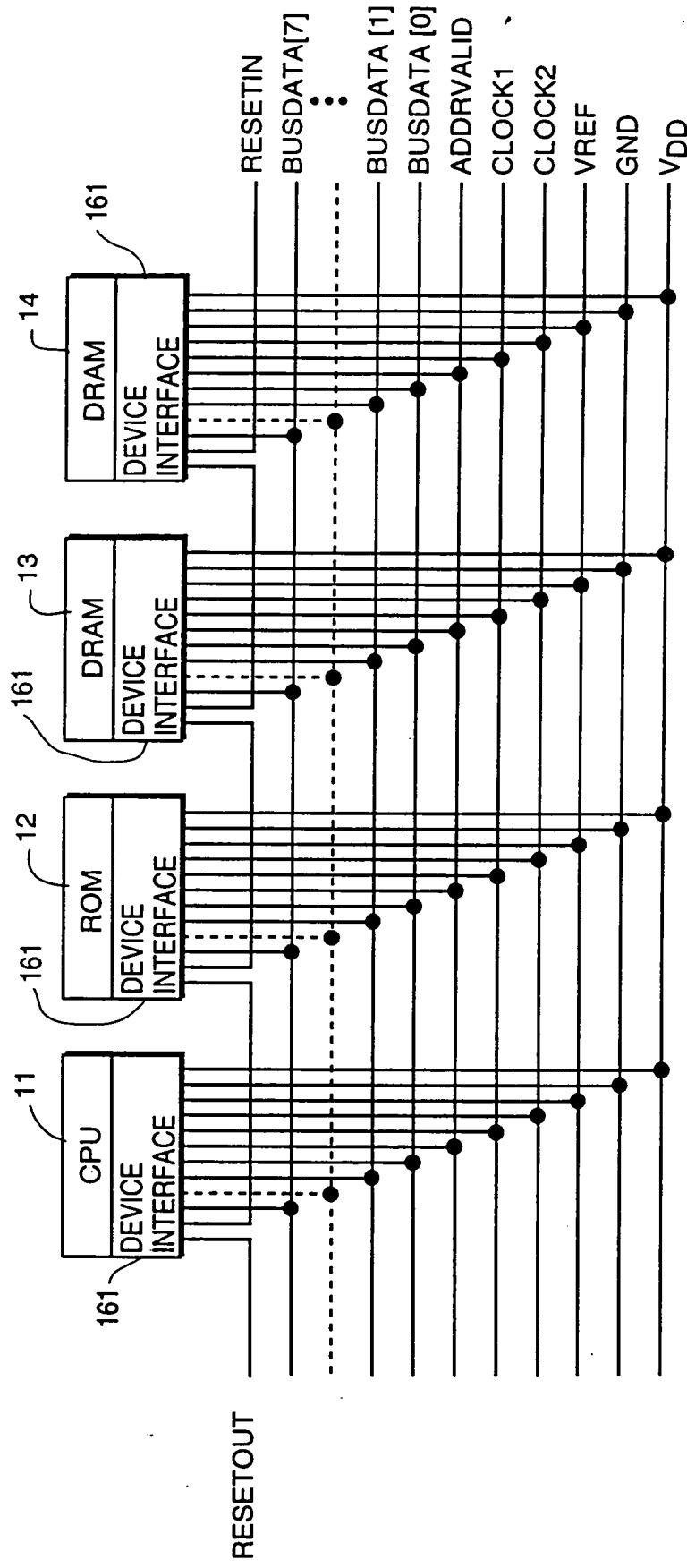
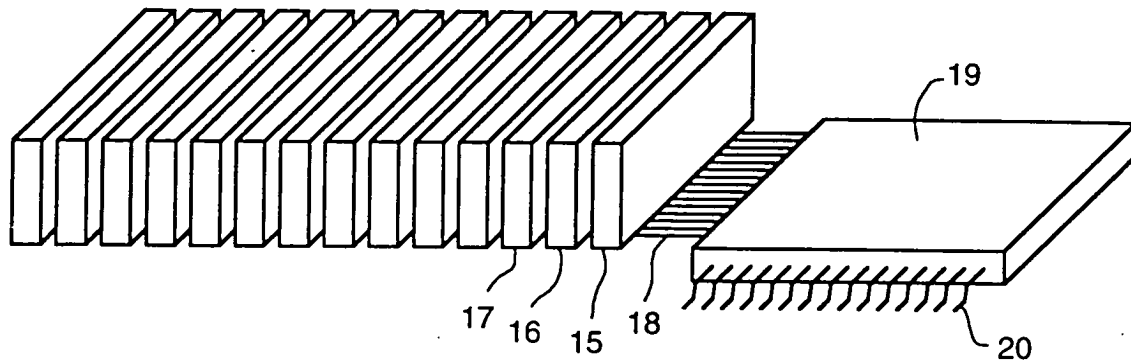


FIG 3



REGULAR ACCESS

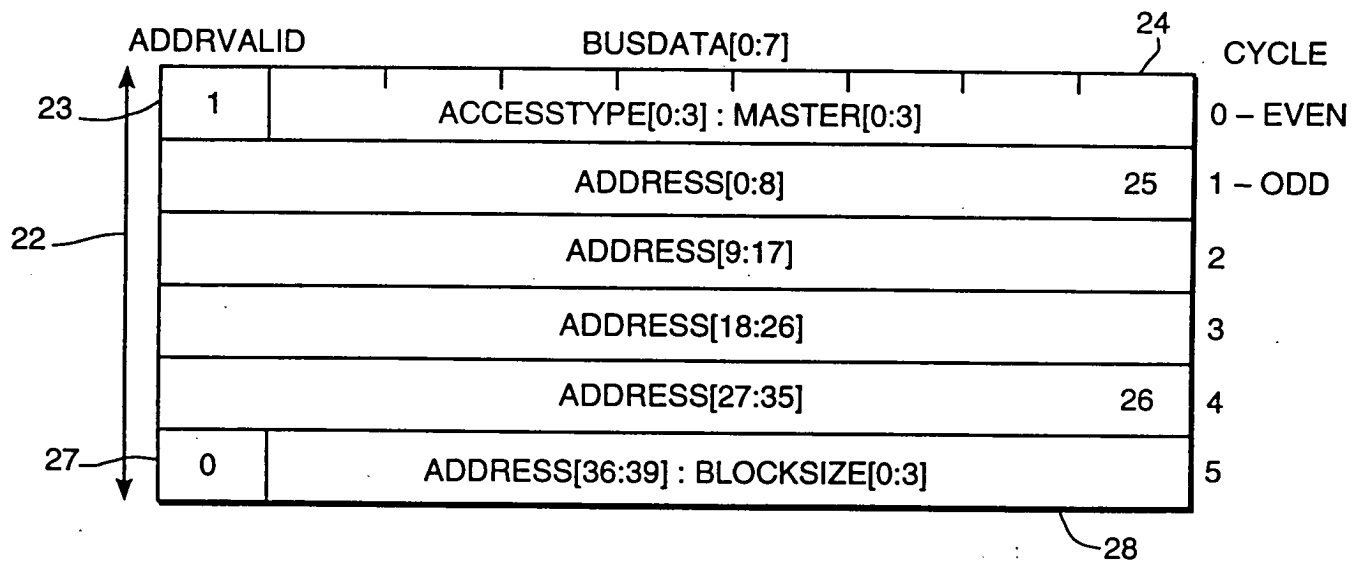


FIG 4

REJECT (NACK) CONTROL PACKET

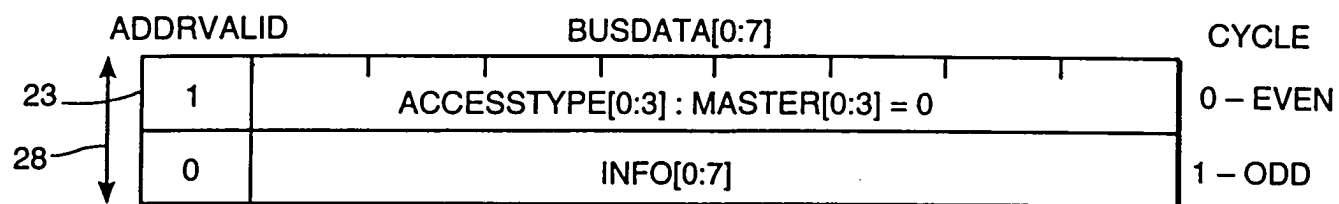


FIG 5

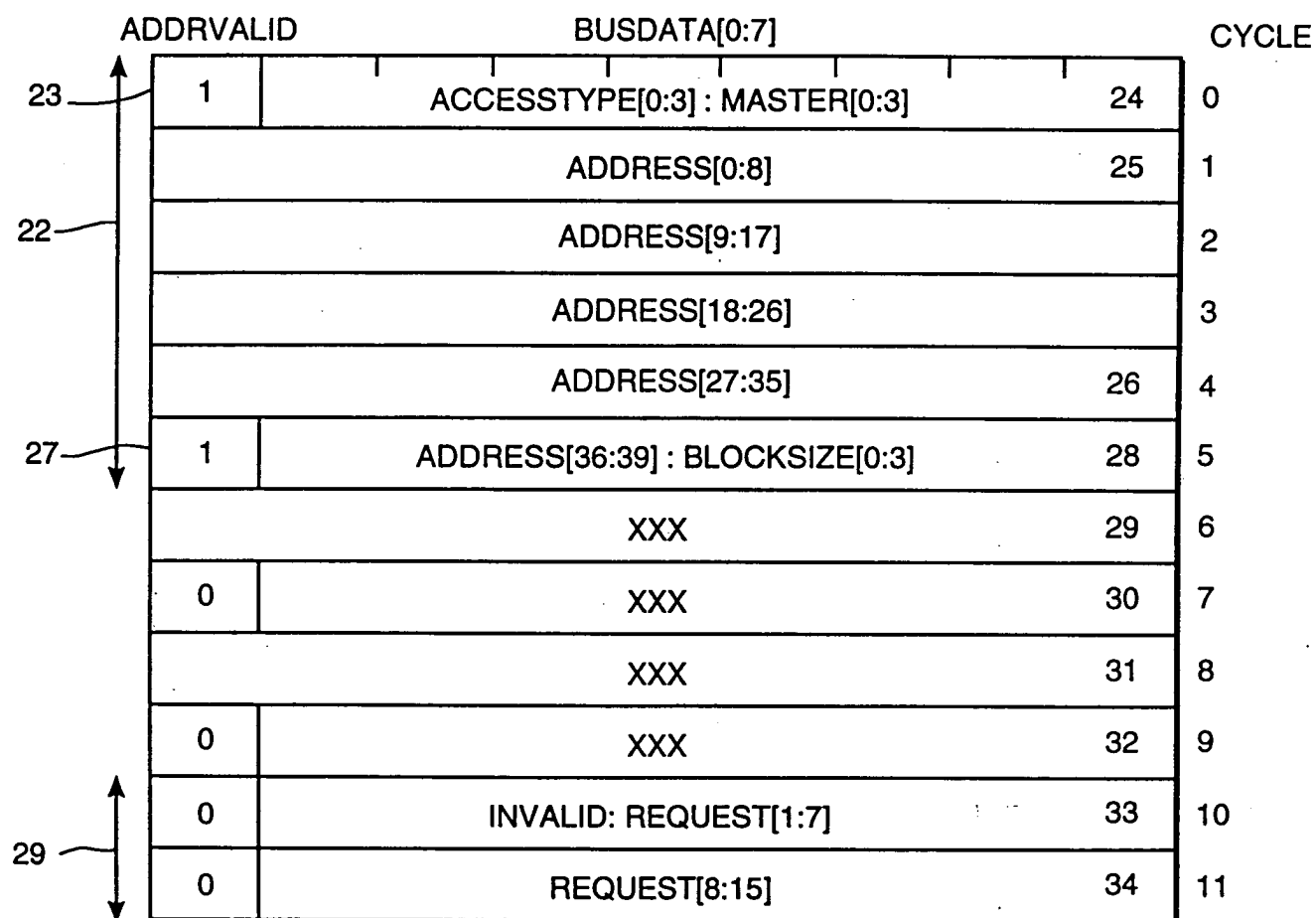
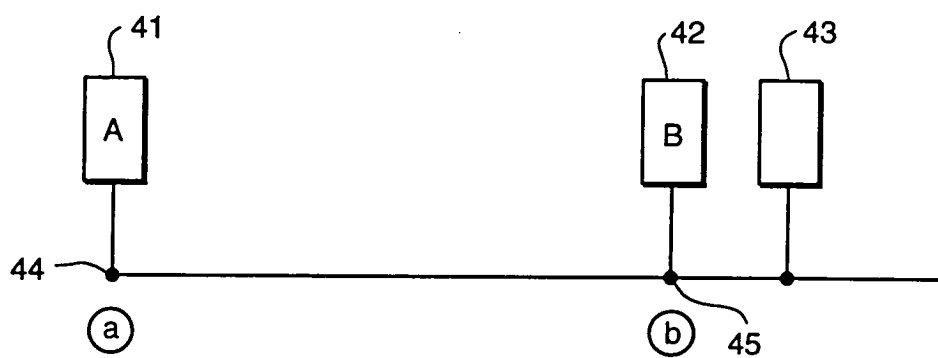


FIG 6



FIG_7A

VOLTAGE LOGICAL
VALUE VALUE

2 0

$V(a)$ 1.5 1
AT 44

1 >1

$V(b)$ 0 1
AT 45

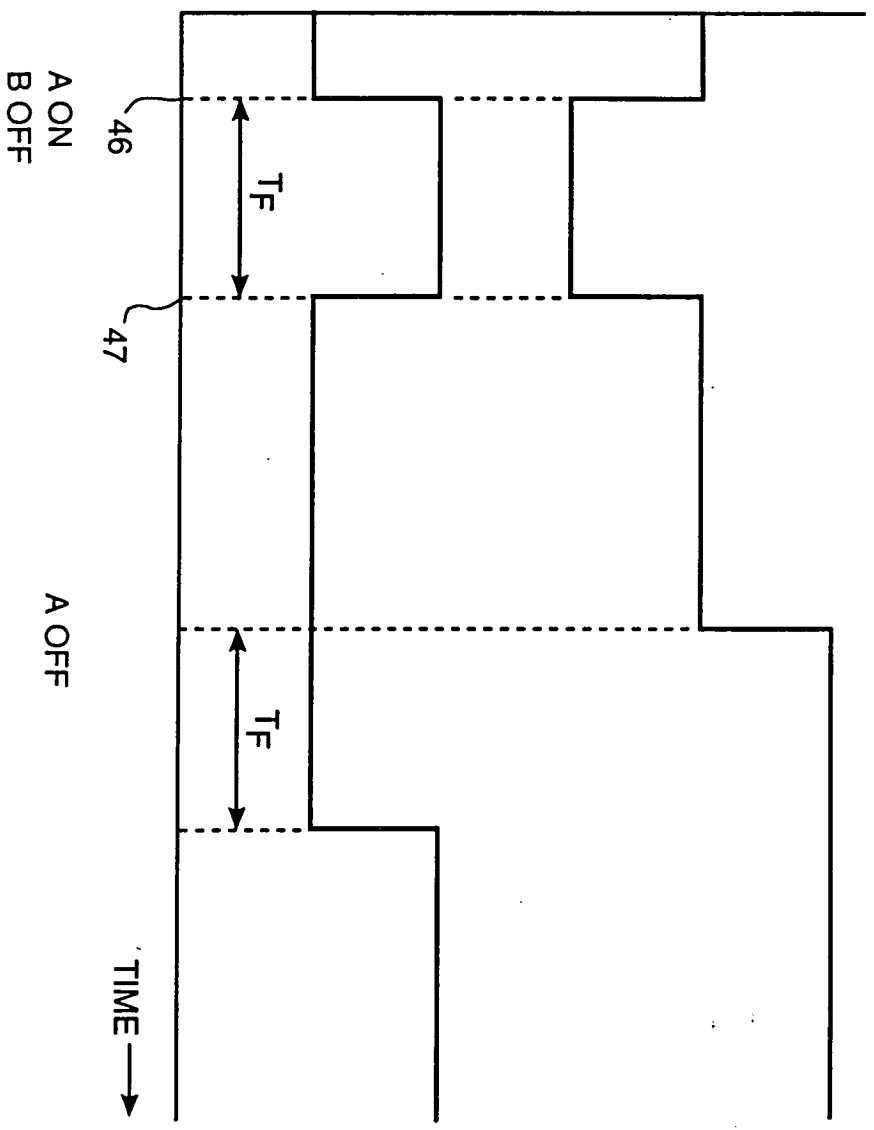
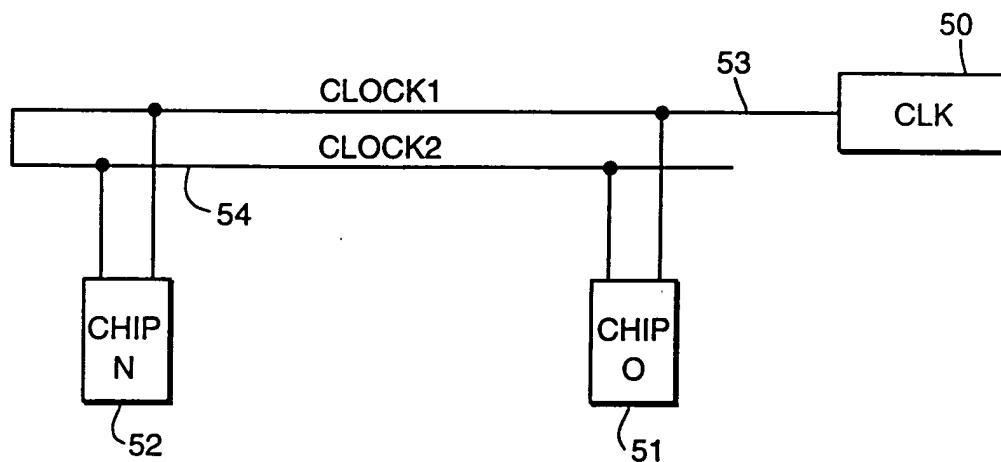
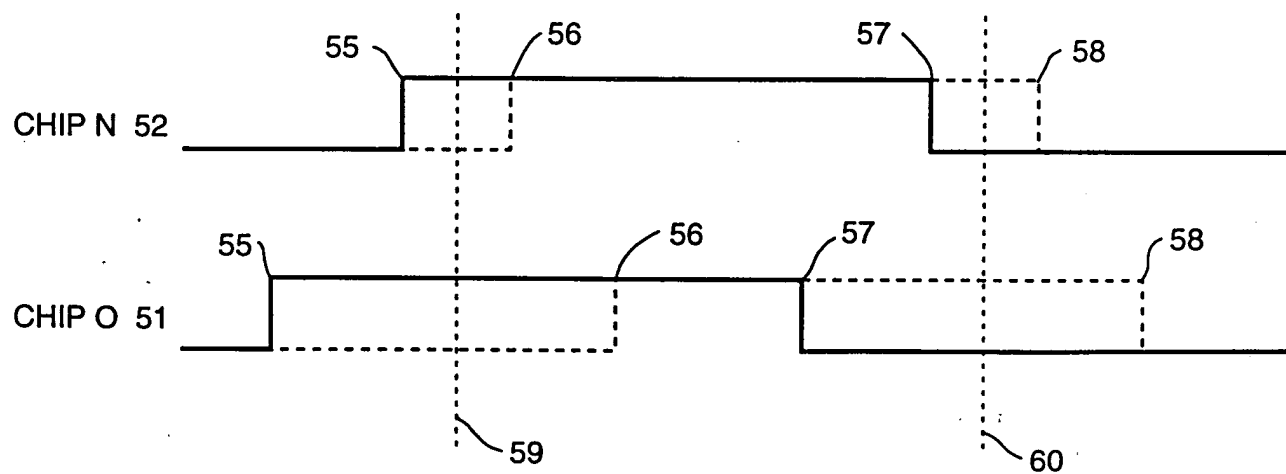


FIG 7B

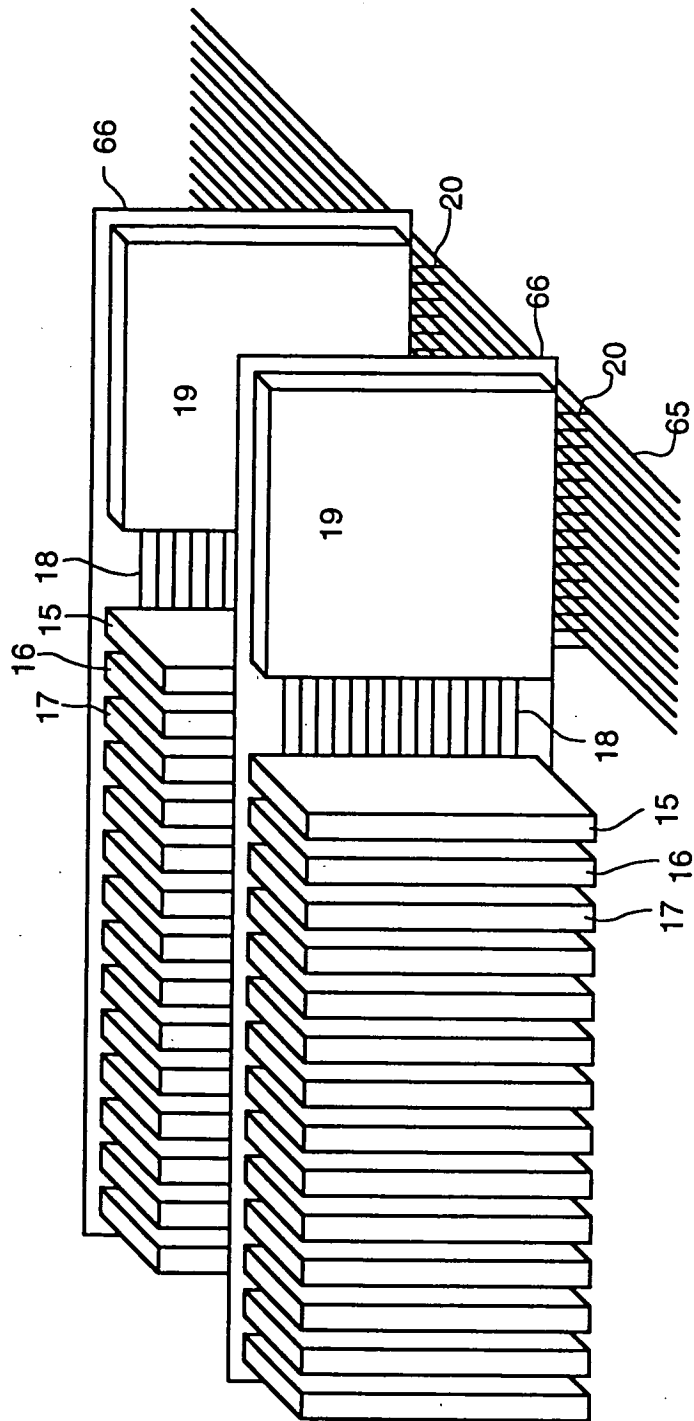


FIG_8A



FIG_8B

FIG. 3



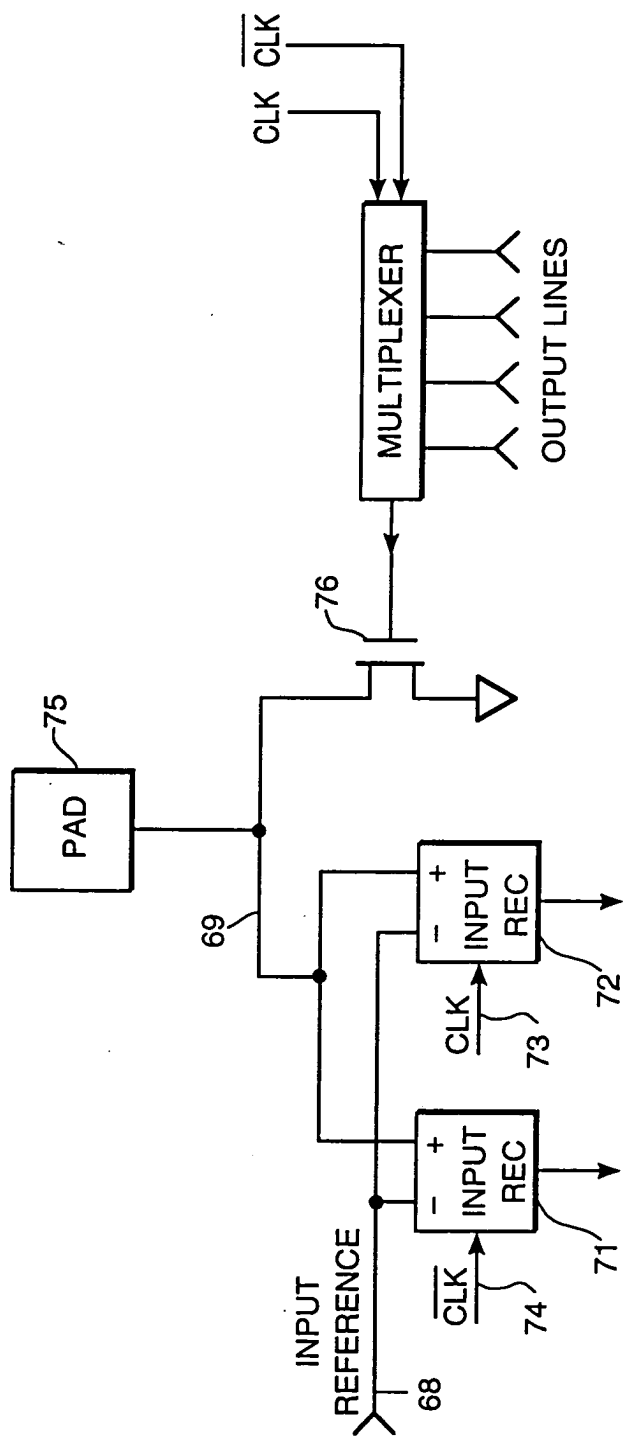


FIG. 10

FIG. 11

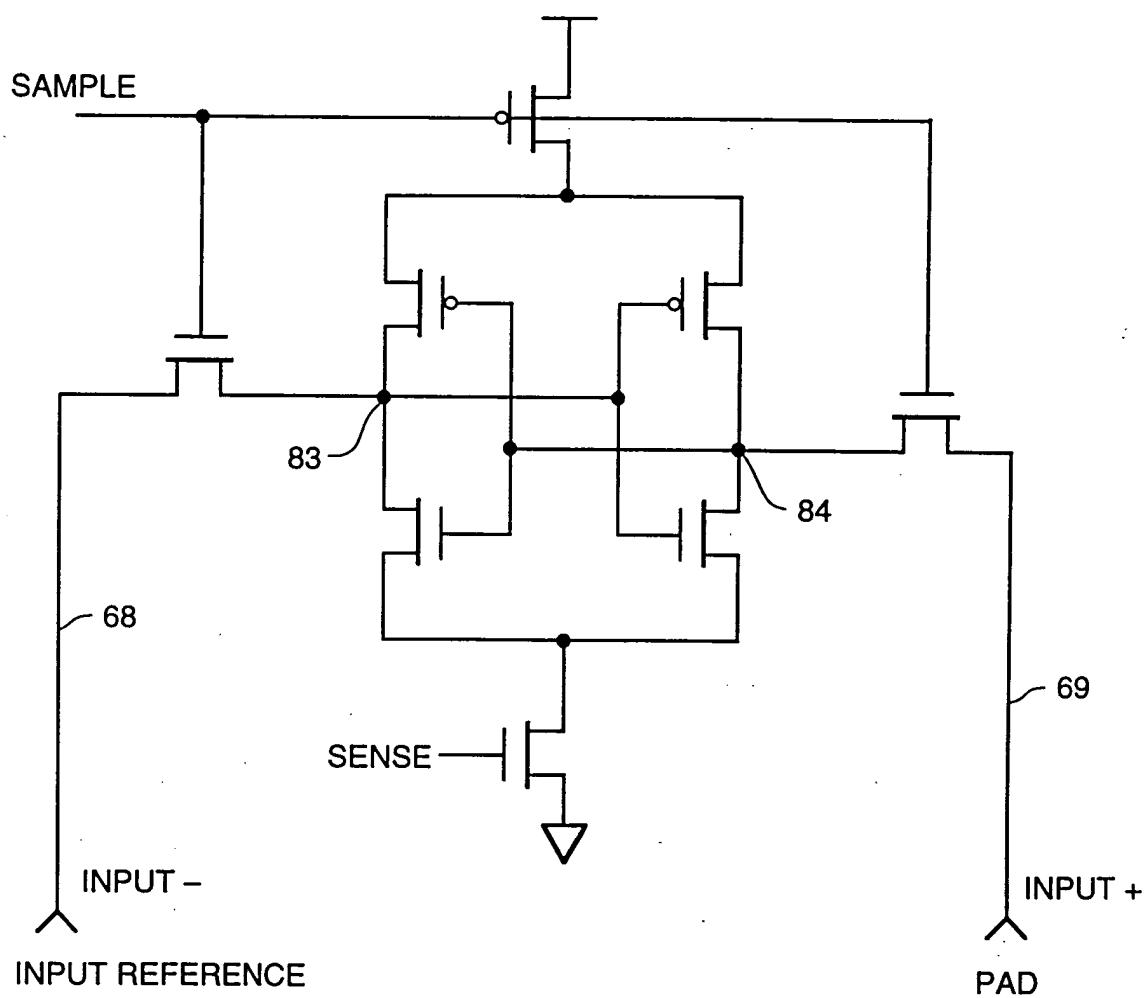


FIG 12

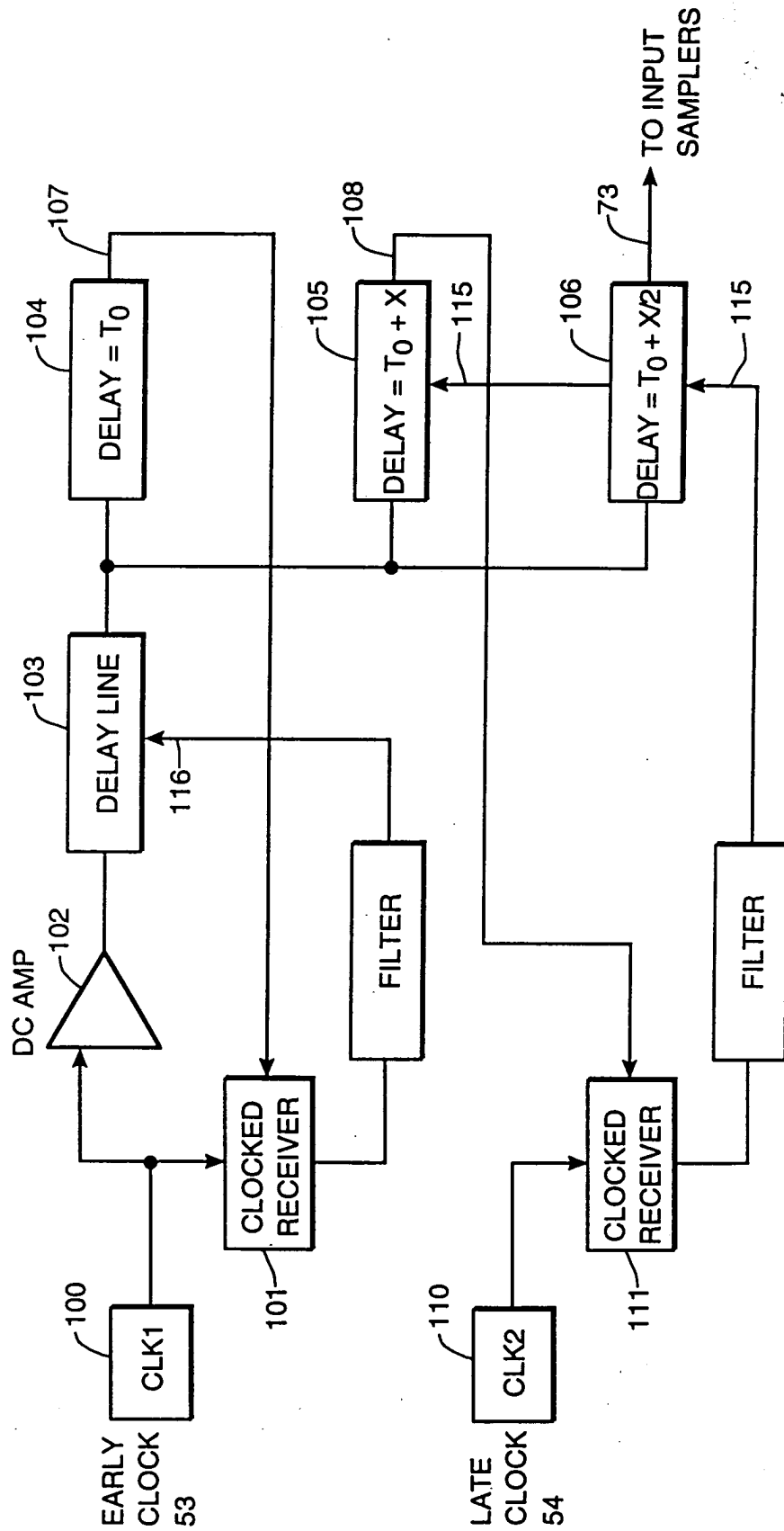
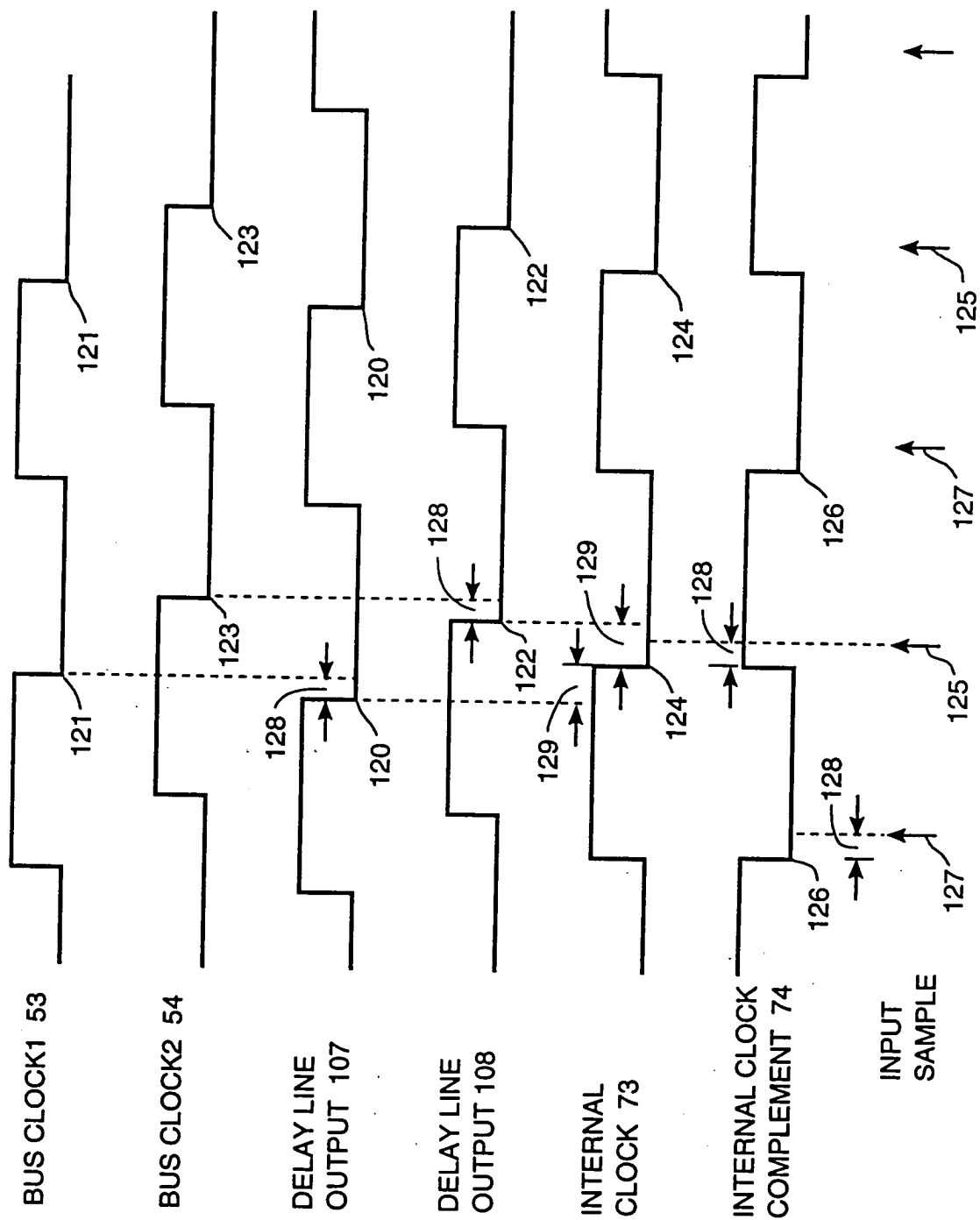


FIG 13



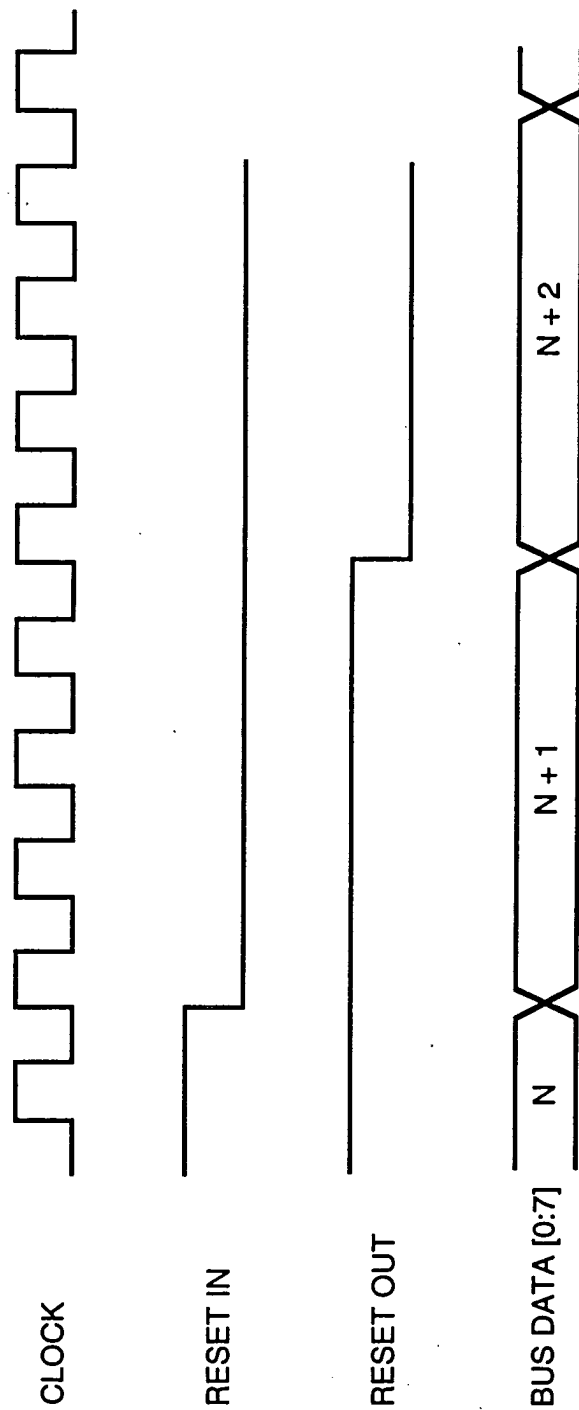
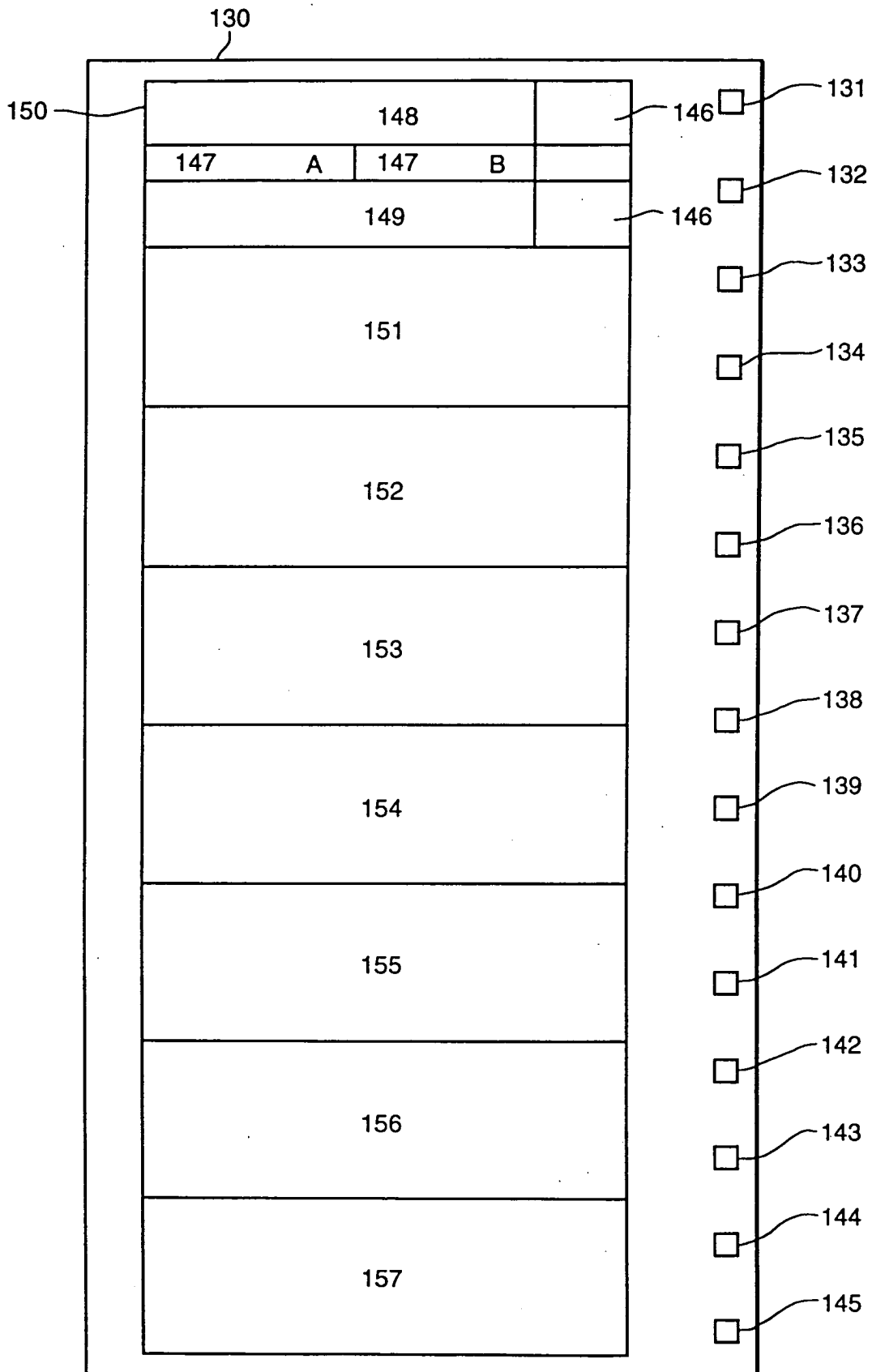


FIG 14

FIG 15



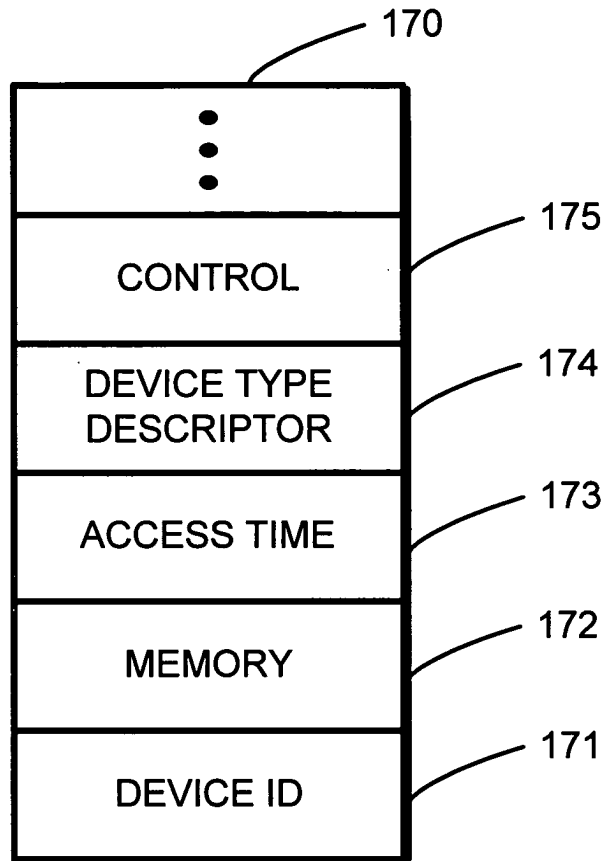


FIG. 16